THE DESIGN OF 7NM FIN FET BASED SRAM USING CADENCE

[1]Dr. John Paul Pulipati, Principal, [2]Gadi Sanjeev, [3]D. Thirupathi,
[4]Chandan kumar Roy
[1]principal@mrce. in,Malla Reddy College of Engineering
[2] Assistant Professor, Dept. of ECE,Malla Reddy College of Engineering
[3]Assistant Professor, Dept. of ECE,Malla Reddy College of Engineering
[4]Assistant Professor, Dept. of ECE,Malla Reddy College of Engineering

Abstract— An envisaged chronological development has been seen in electronic industry since from the invention of Radio Transistor to the present battery portable devices. There are various semiconductor devices included with primary memory cells like SRAM. The SRAMs are ubiquitous in new era of VLSI Technology but the challenge arrives when we want to implement it by predictive nodes like 7nm,5nm and beyond it. According to Moore's law, transistor's size shrinks by adjusting a greater number of Fins. Fin FET based SRAMS allows considerable area and power reduction and its process variations will have a great impact on parameters like fin count, thresh hold Voltage, Effective Oxide Thickness, off state current, drain current and Sub threshold Swing. This paper discusses about 7nm bulk Fin FET SRAM with different observations like access time of two 6T SRAM cell, thermal stability and noise ratio. The percentage of operational failure can be minimized based on SRAM cell stability and analyzed by Cadence tool. The TCAD simulation shows that compared to planar SRAM, soft error rate in Fin FET SRAM is considerably decreased. The simulations results show that if we increase the PD transistor fins and the Reverse Static Noise Margin can be obtained with the reduced power supply.

Index terms-Bulk-Fin FET, Cadence, Fin FET, SRAM, Soft Error Rate, Static Noise Margin, Shorted Gate and Thermal Stability.

I. INTRODUCTION

The portable applications requiring low power dissipation and high throughput such as note book computer, personal digital assistants and some portable communication devices. In a rapidly developing field of CMOS design, the technology nodes have been changing its strategies and monitoring the parameters asper requirement to the customers [1]. But now a days, many customers are complaining that the product speed is not to the desired level it means the device is running with low frequency. It's difficult to determine because it's all about process variations [2]. Memory occupies more than 70 percent of area in today's system on chip, its tendency remains to be rises in coming years. The technology is scaling the bulk MOSFET, faces a variety of challenges and which lead to become more intense leakage. The Digital Signal Processors, Multiplexers and many computing devices are stacked to the memory modeling. Owing to this fact, weather it is planar or nonplanar device we primarily focus on speed, cost by balancing the parameters like channel length modulation(lambda),.

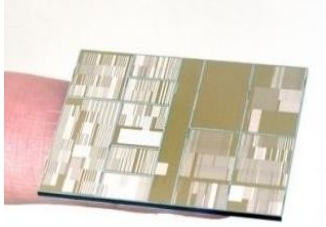


Fig1.The 7nm Chip

ISSN (PRINT): 2393-8374, (ONLINE): 2394-0697, VOLUME-4, ISSUE-12, 2017
DOI:10.21276/ijcesr.2017.4.12.41

The research centers and several companies has released the details on 7nm as an initial step for efficient development with a target of 4nm by 2025.In a simple way we can say that lower nanometer number gives higher efficiency and better performance [3].If we compare 14nm to 7nm node technology, we can see notable changes in mobile industries which are only depend on battery power consumption which was the main problem and the switching speed can be increased from 20% to 50% with best resolution screen [3]. "The SRAM Critically affects the total power of Soc and occupies a greater portion on it". The power reduction can be reduced with reducing operating voltage. The SRAM cells are highly susceptible to variations in Thresh hold voltage *V*th.

II. THE HISTORY OF SRAM

The First Integrated circuit of SRAM was sold around 1970 about 50 years ago and Till about 20 years ago SRAM still only exists as standalone Integrated Circuits .It was one of the biggest IC market on the planet at that time The Static RAM is the cache memory consist of a Latch which is the fundamental building block of any memory element[5].It is designed with the two cross coupled CMOS inverters

,the reason for using inverter is it exhibits higher noise margin levels. In a simple way it acts like a one -bit storage cell called Flip Flop which is a Bi stable. It consists of two access transistors for reading and writing the data [6]. Let us consider the differences between DRAM and the SRAM DRAM, the important differences are bit lines and periodic refreshment.

To understand what and how actually to select an SRAM for any processors, consider ISSI manufacture of parallel interface. The ISSI IS62C1024AL/IS65C1024AL is a low power, 131,072-word by 8-bit CMOS static RAM. It is fabricated using high-performance CMOS technology which is highly reliable process coupled with innovative circuit design techniques, gives higher performance and low power consumption devices.

Fig2.An 8bit low power CMOS static RAM

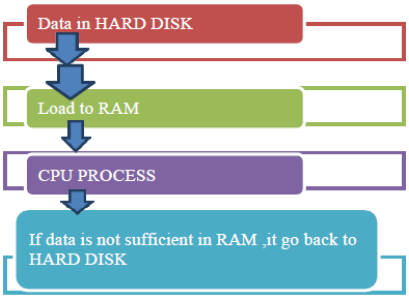


Fig3.Loading a program from memory to CPU

A.THE ARCHITECTURE OF EXISTED CMOS STATIC RANDOM-ACCESS MEMORY

The write ability of a SRAM can be achieved by adjusting the Thresh hold Voltage VDD to a certain level and the virtual VSS. The configuration of the cross coupled inverter plays a vital role in all the existing bit cells but can't incorporate process variation tolerance for improving the thermal stability

of an SRAM cell [8]. By adding the extra Transistors, we can decouple the read and write operations. Under PVT variations, the stability of cross coupled inverter will decide the SRAM operation. However, the sizing of the device at low supply voltage cannot affect the cell stability of SRAM [9].

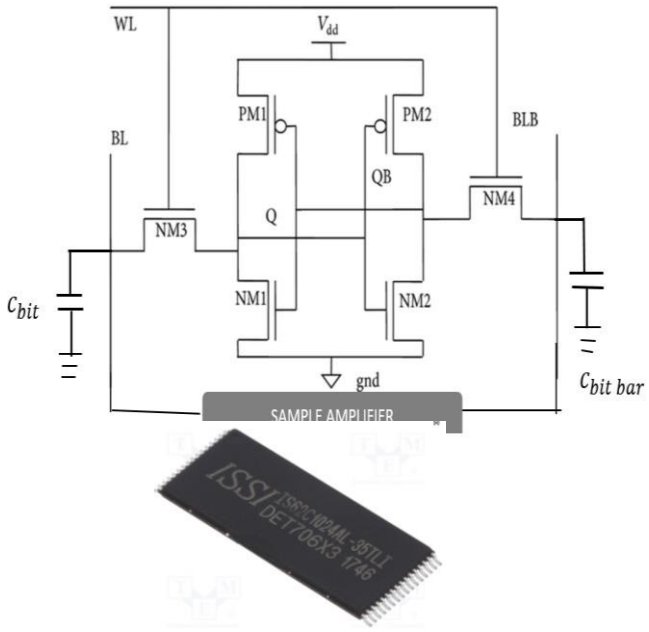


Fig4.The 6T CMOS Static RAM

ISSN (PRINT): 2393-8374, (ONLINE): 2394-0697, VOLUME-4, ISSUE-12, 2017
DOI:10.21276/ijcesr.2017.4.12.41

the above figure

(i).PM1 & NM1 is CMOS Inverter1,PM2 & NM2 is CMOS Inverter 2 which are cross coupled toact as memory.

(ii) Most RAMs are built so that all cells in the same row are activated [6]. If Word line is HIGH(1) then Bit Line(BL) &Bit Line(BLB) bar accesses read and write Transistors, if wordline is zero then the bit ,bit bar are in stan by mode or hold state.

(iii)TheBit Line(BL),Bit Line Bar(BLB) are access for write and read for input and output respectively[7]. (v).TheSample amplifier act as comparator compares two bit values if bit line bar value is '0' then it gives output as HIGH (1) or else LOW (0).

The row decoder,the precharge capacitor is used for read and write operation and sense amplifier which connected to column mux act as comparator which compares bit and bit bar values and gives output value based on bit bar[6]. But Still there exist issues like Soft Errorsbecause of induced alpha particles leakage currents[4].

The design Tradeoffs of CMOS SRAM

Stability and Static Noise Margin: The cells ratio of Transistors will decide the stability of a SRAM cell and good Static Noise Margin depends on the cell stability.

Soft error Rate: In CMOS SRAM, Soft Error Rate increases as the cell capacitance and power supply voltage decreases. Due to the relativity of small amount of charge at storage nodes, the SRAM'S are particularly sensitive to radiation induced soft errors emitted from trace amounts of Uranium in soldering [11]. The NBTI occurs with a negativegate to source voltage and increases PMOS threshold voltage, slowing down logic gates in digital design, causing mismatch in Analog design and reducing read and hold noise margins for SRAM and PBTI (Positive Bias Temperature Instability) has not caught much attention mainly due to their ignorable impact for thin gate oxide. PBTI happens when positive gate to source voltage is applied and weakens NFETs similarly as NBTI degrades PFETs[11].

THE ARCHITECTURE OF PROPOSED 7 FIN FET BASED SRAM

The AMD was the first company to launch 7nm processor chips. The term node is used by the

semiconductor industry to characterize major targets in their manufacturing road map[12].The7-nanometre chip can hold up to 20 billion transistors. The development of the chip began in 2014 as a part of IBM's $3 billion research program. The research of the program was carried out by SUNY Polytechnic Institute's College of Nanoscale Science and Engineering [11].

A. The 7nm Fin FET Node

The Fin FET manufacturing Technology was used by almost all flagship mobile chipsets in the market. Now, moving to 7nm is another shrink down which usually give better Transistor Density with improved power efficiency. But the 7nm chips are very expensive and so chip design is cost [10]. To Understand the fins arrangement in Static Random- Access Memory, lets analyze the 3D view of a Tri Gate Fin FET.

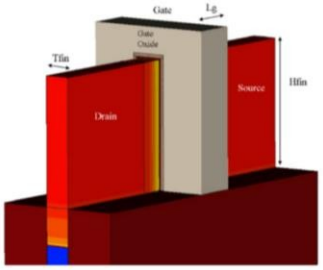


Fig5. The 3D View of a Tri-Gate Fin FET

The Fin FETS are the 3D device focus on the corners and edges. The gate dielectric field wrap around the Fin and gate metal.The SRAM device is selected from the Process Design Kit it models the process for design tools based on certain assumptions The BSIM CMG compact model is used for simulating the device static Behavior [13]. We Apply Gate voltage at corners 'Vg' at corners which is greater than the gate voltage at side walls of the gate. The Fin FET device

consists of a thin silicon body, with thickness T fin wrapped by gate electrodes and device is termed quasi-planar as the current flows parallel to the wafer plane. we define a Fin FET technology by their effective gate lengths.So, it is set to be 7nm in 7nm Fin FET device models[13]. The channel is formed perpendicular to the plane and the effective gate length Lg is twice as large as the fin height 'H fin' which is given by following expression

The minimum Width of the Fin FET connecting N number of fins with Channel width of W is given by The Fins connected are tall,narrow and Gate wraps around the fins on tops and sides Because of narrow fins gate electrostatic integrity is enhanced. The Fin pitch and CPP determines the Transistor density [14].

WORKING METHOD

A. The 7nm Fin FET 6T SRAM cell working The SRAM cells may generally be classified according to the manufacturing configuration of the load elements used in the cells. The Fin FET based design is the low power working due no body biasing and less power supply because the Gate wraps around Fins of Source and Drain leads reduction of leakage current and charge discharge and so many issues[15].

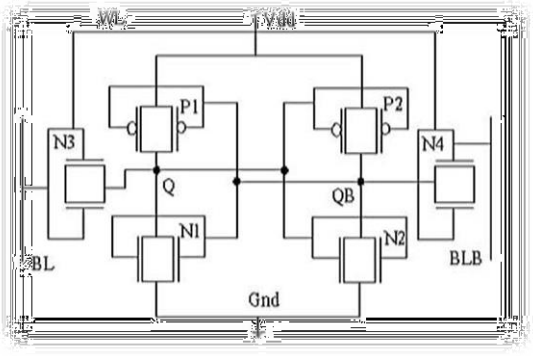


Fig6.The shorted Gate of 6T FinFET SRAM

The working of Fin FET SRAM is almost same as 6T CMOS SRAM but leakage current and power dissipation is less in Fin FET SRAM and E-memory (FLASH) MUGFET based helps in cell issues, reduced leakage current, lesser device mismatch. Fin FET SRAM requires low power due to no body biasing.

B. Fin Count Adjustment

1.The Pull UP, Pull Down and Pass Gate transistor gates are adjusted with the ratios of "111" and "121"

2.The "111" configuration is for to maintain minimum cell area and "121" configuration is for read and write stability.

3.In order to reduce write operational failure, the adjustment of Pull Up ratio with write assist circuit is mandatory[17].

B. Layout Designs of CMOS SRAM and Fin FET SRAM

The Transistor height for a Fin FET device is proportional to (NFIN − 1) • PFIN, where NFIN denotes the number of fins obtained and PFIN is a process related geometry that restricts the minimum space between two adjacent fins and NFIN •PFIN as the transistor height. The Transistor width, on the other hand, is determined by contact-related design rules (i.e., WC and WG2C) and the channel length.[17]. The design rules are identical in CMOS and Fin FET technologies for wires and contacts.

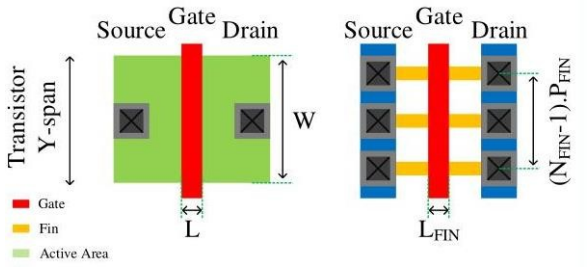


Fig7.The Planar CMOSSRAM Fig8.The Fin FET SRAM

V. SIMULATION RESULTS

In SRAM, the Vth variation is crucial due to its direct impact on the unit cell read and writes stability,The Work Function is mainly adjusted to fine-tune the Vth value which is an effective parameter for the memory unit cell stability. Increasing Vth the cell becomes more stable during read and write operations[17].

The Transistor Density Calculation

The Transistor Density is calculated in terms of MTr/mm^2 which stands for millions of Transistors per square millimeter.[19]

Transistor area calculation for CMOS SRAM and Fin FET SRAM

ISSN (PRINT): 2393-8374, (ONLINE): 2394-0697, VOLUME-4, ISSUE-12, 2017
DOI:10.21276/ijcesr.2017.4.12.41

Let us consider layouts CMOS and SRAM from Figure 8 and Figure 9,

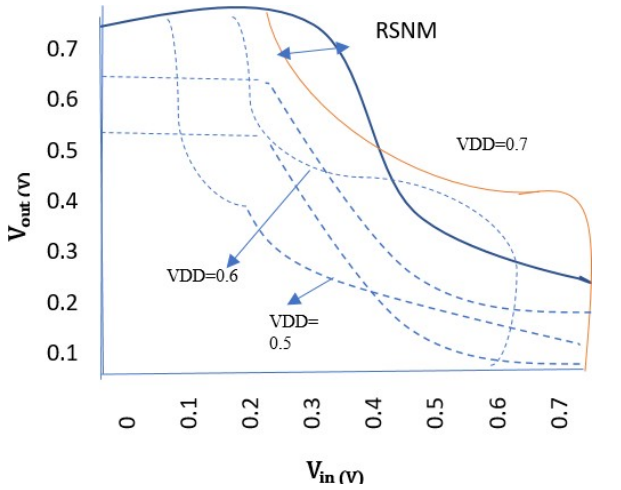
X-Span(Transistor Height) =31.5 nm,Y-Span=21nm. Length of the Fin(Lfin)=7nm.

The CMOS width =21nm.

The Fin FET Height (Hfin)=14nm, Fin Pitch =10.5nm.

And $The\ area\ is\ given\ by\ A$ = [W] $*$ 10.5nm A=56nm [18].

The Reverse Static Noise Margin(RSNM)



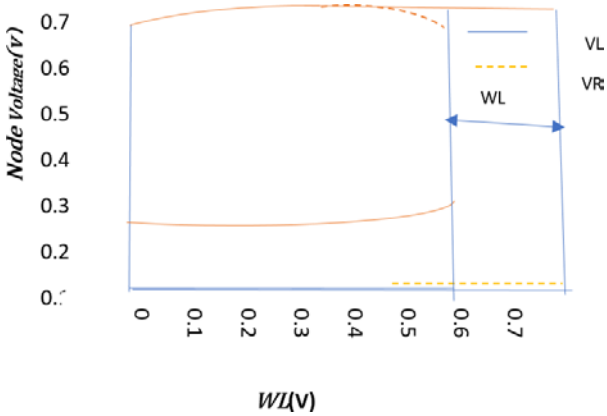
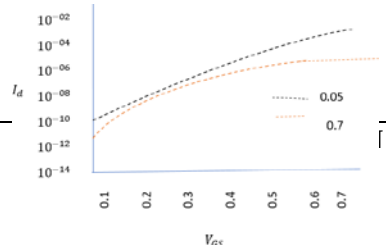


Fig 9(a).The variation of Vout with respect to VDD at 0.5,0.6 and 0.7 volts Fig9(b).WORDLINEWRITE MARGIN(WLWM)

Above Observations from TCAD Tool



From the Figure9(a),read stability can be measured by RSNM, if RSNM is negative then read stability is unstable.From Figure 9(b),Word Line Write Margin has ability to lower the Word Line(WL) voltage.

Drain Current Vs Gate to source voltages of 6T Fin FET SRAM

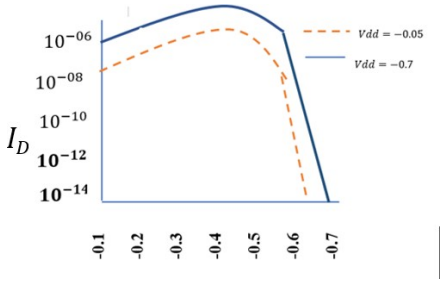


Fig10(a). The N fin FET 6T FinFET SRAM Fig10(b)The P FinFET of 6T FinFET SRAM

Apart from the all characteristics of SRAM ,7nm node,it is necessary to analyze the thermal profile of a FinFETdevice irrespective of its size of memory used in processors. The 3D FEM simulations are used to

VI OBSERVATIONS

TABLE I

The supply voltage @VDD=0.7v to 7nm Fin FET SRAM

S.No	Parameter	N FInFET	P FinFET
01	Vdss(sat)	0.7v	-0.7v
02	Vth	0.282v	-0.266v
03	Ioff	72Pa/µm	0.6Pa/µm
04	SSwing	63mv/dec	65mv/dec
05	DIBL	25mV/V	32MV/V

TABLE II

Bulk Si Fin FET DC Performance parameters

extract thermal resistance (Rth temperature size (ΔT) [22].

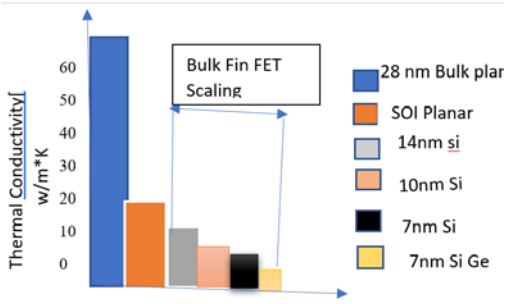


Fig1.:Thermal Profile of 6T Bulk FinFETSRAM

On a single Si channel fin, there is a 20% improvement in *Thermal Resistance*(*Rth*) with decrease in device dimension nodes which degrades the device heatdissipation [23] as shownin Fig10.

From above observation it was showing that instead of running device with Silicon substrate,if we add other materials likeGermanium(Ge),Indium-Gallium-Arsenide(In-Ga-AR),thethermal conductivity gradually decreases thus by providingbetter cooling,The TCAD simulations indicating that the SER rate in Bulk Fin FET based SRAM is better than planar SRAM.

VI OBSERVATIONS

TABLE I

The supply voltage @VDD=0.7v to 7nm Fin FET SRAM

	Parameter	N FInFET	P FinFET
	Vdss(sat)	0.7v	-0.7v
	Vth	0.282 v	-0.266v
	Ioff	72Pa/µm	0.6Pa/µm
	SSwing	63mv/dec	65mv/dec
	DIBL	25m V/V	32MV/V

TABLE II

Bulk Si Fin FET DC Performance parameters

	Parameter	N FInFE T	P FinFET
	Lgate	20nm	20nm
	EOT	Inm	1nm
	Hfin	32nm	32nm
	Tfin	6.5nm	6.5nm
	DIBL	25mV/ V	32MV/V
	FinDoping	2*10^1 5cm^-3	2*10^15cm^-3
	WF	4.45 eV	4.78 eV
	Gate Cut Min.Width	17nm	17nm
	Source to drain Trench(SDT)	17nm	17nm

TABLE III

The measured Alpha Emission rates used for Si processing .

S.no Materials AlphaEmission Rate counts/hr/cm^2

01 Process wafers 0.0006-0.0014

02 Polymers Used in Integrated FanOut <0.0008

03 Lead(Pb) 7.2-0.002

VII. CONCLUSION

The following results shows that, the variation of Thresh hold voltage to obtain Reverse Static Noise Margin, we have to increase the Pull-Down Transistor's ratio. Even at supply voltage0.5 VDD, the read and write operations are stable at Transistor fins configurations [19]. The Soft Error Emission was considerably decreased by Integrated Fan Out Technology.

VIII. FUTURESCOPE

If we Compared to 10nm Fin FET process, TSMC'S 7nm Fin FET features 1.6X logic density,20% speed improvement and nearly 40% power reduction andalso launched two separate 7nm Fin FET Tracks.one for mobile applications and other for high performance computing applications [17]. The Intel Xenon GP- GPU (General-Purpose Graphics Processing Unit) is the first 7nm chip arriving in 2021 and it will deliver about 20% improvement over its predecessors [12]. The Intel is overlapping both the 10nm and the 7nm featuring Xenon architecture or Tiger Lake architecture in 2021

ISSN (PRINT): 2393-8374, (ONLINE): 2394-0697, VOLUME-4, ISSUE-12, 2017
DOI:10.21276/ijcesr.2017.4.12.41

and also 7nm will take center stage in 2022

IX. REFERENCES

[1].http://gvpcew.ac.in/LN-CSE-IT-22-32/ECE/4-Year/LowPower-VLSI-Unit1.pdf

Need for low power design.
[2].https://www.wisegeek.com/what-are-primary-storage-devices.htm

The primary storage devices

[3].https://hal.archives-ouvertes.fr/hal-01558775. Technology Road map and improved Performance of 7nm technology.

[4].http://www.ieeexpert.com/vlsi-2016/full-swing-local-bitline-sram-architecture-based-22-nm-finfet-technology-low-voltage-operation/

The SRAM on System On Chip.
[5].https://www.bing.com/videos/search?q=backend+vlsi+sram+memory&&view=detail&mid=43E43A1141 7A347A0C0543E43A11417A347A0C05&&FORM= VRDGAR

The basic concepts in 6T SRAM Transistor
[6].www.cse.scu.edu/~tschwarz/coen180_04/LN/sram. htm

The row and column decoder selection in SRAM array
[7].https://www.youtube.com/watch?v=k5VBJcUcaW U

The SRAM memory to access transistor and vice versa logical operation
[8].http://www.iosrjournals.org/iosrjvlsi/papers/vol8 - issue1/Version-1/E0801014346.pdf6

The overall theoretical analyzation of SRAM circuit.
[9].https://shodhganga.inflibnet.ac.in/bitstream/10603/ 141452/10/10_chapter%202.pdf

The design of an 6T SRAM Circuit
[10].https://www.bing.com/videos/search?q=7nm+technology&&view=detail&mid=AF86E0D0A60BC4FE2 E14AF86E0D0A60BC4FE2E14&&FORM=VRDGA R

A deal with 7nmTechnology
[11].http://goofyygadgets.blogspot.com/2015/07/ibm- unveils-first-7-nm-chip.html

The IBM 7nm Microchip Technology.

[12].https://www.technewstoday.com/intel-is-launching-7nm-processors-in-2021

The Intel technology path towards 7nm node.
[13].https://www.bing.com/videos/search?q=7nm+pre dictive+design+kit

An Introduction to Process Design Kit
[14].https://www.nist.gov/system/files/documents/201 7/04/04/zeitzo.f.pdf

The schematic view and key dimensions of 7nm Fin FET.

[15].https://www.accentsjournals.org/PaperDirectory/J ournal/IJACR/2015/12/4.pdf

The circuit of 6TSRAMFin FET
[16].https://www.sciencedirect.com/science/article/pii/ S002626921630026X

Fin count adjustments in 7nm Fin FET
[17].https://www.researchgate.net/publication/3308815 15

Low_Power_7_nm_FinFET_based_6TSRAM_Design The Fins of SRAM cell adjustment.
[18].https://www.slideserve.com/ilori/fincacti-architectural-analysis-and-modeling-of-caches-with-deeply-scaled-finfet-devices

The Layout area calculations.
[19].https://www.techcenturion.com/7nm-10nm-14nm- fabrication

TheTransistor Density calculation by Intel Technology.
[20].https://www.researchgate.net/profile/Saurabh_Sinha9/publication/301830005_ASAP7_A_7nm_finFET_predictive_process_design_kit/links/573b59aa08ae9f7 41b2d7f8b/ASAP7-A-7-nm-finFET-predictive-process-design-kit.pdf?origin=publication_detail

The Technical parameters observations.
[21].https://www.researchgate.net/profile/Penerbit_Akademia_Baru/publication/330881515_Low_Power_7_ nm_FinFET_based_6T-SRAM_Design/links/5c5990f845851582c3cfec97/Low w-Power-7-nm-FinFET-based-6T-SRAM-Design.pdf?origin=publication_detail

Drain current amd collected charge.
[22].http://edpsieee.ieeesiliconvalley.org/edp2013/Paps ers/4-3%20FINAL%20for%20Raymond%20Leung.pdf

The observation of TCAD simulations and characteristics using 7nm node using cadence tool.
[23].https://www.scihub.tw/10.1109/IEDM.2015.7409 6780

The Self Heating Technique to reduce heat dissipation in Fin FET.

[24].https://www.sci-hub.tw/10.1109/IRPS.2018.8353584

The Alpha emission rates of several process materials and package materials using INFO (Integrated Fan Out) and Redistribution Layers.